Fall 2018

ECE 251 - Digital Design

Jacob Savir

ECE251

1. Course number and name: ECE251 Digital Design

2. Credits and contact hours 3 credits; 4 contact hours.

3. Instructor's or course coordinator's name Jacob Savir

Text book, title, author and year Alan B. Marcovitz, *Introduction To Logic Design, 2nd edition (or higher)*, McGraw-Hill, ISBN # 0-07-286516-4.

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   a. other supplemental materials: Class notes

4. Specific course information
   a. Catalog Description: The design of combinational and sequential logic circuits used in digital processing systems and computers. Basic register transfer operations are covered. Topics include Boolean algebra, minimization techniques and the design of logic circuits such as adders, comparators, decoders, multiplexers, counters, arithmetic logic units, and memory systems.
   b. prerequisites or co-requisites: Phys 121
   c. indicate whether a required, elective, or selected elective: required

5. Specific Course Learning Outcomes (CLO):
   I. Are able to use Boolean Algebra.
   II. Are able to minimize Boolean functions.
   III. Are able to design digital circuits with gates, latches and flip flops.
   IV. Are able to analyze digital circuit in a multitude of possible applications.

   Relevant student outcomes (ABET criterion 3):

   (a) an ability to apply knowledge of mathematics, science, and engineering (CLO I, II)
   (e) an ability to identify, formulate, and solve engineering problems (CLO III, IV)
   (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. (CLO III,IV)

6. Brief list of topics to be covered:

   Week 1: Number systems: decimal, binary, arbitrary radix representation.

Week 2: Representation of positive & negative numbers. Two's complement, One's complement, signed-magnitude, Hex, Octal, Ternary. Quick conversion between bases.
Week 3: Gates, truth tables, Boolean algebra, Function simplification.
Week 4: K-maps. Circuit implementation using K-maps. SOP and POS representation. NAND/NOR implementations.
Week 5: Mux, Demux, decoders, code conversion (BCD to Binary, Excess 3 to binary).
Week 6: Hazards, hazard-free design.
Week 7: Function implementation using MSI logic.
Week 8: Latches and Flip-flops: SR, D, JK, T.
Week 9: Counter design, register design, ALU function.
Week 10: Sequential circuits. Excitation function, state table, state diagram.
Week 11: Sequential circuit design with different flip-flops.
Week 12: Asynchronous circuits analysis and design. Excitation function, Flow table.
Week 13: PLDs, ROMs, PLAs, PALs.
Week 14: Review.